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Claims

[c1] What is claimed is:

1.A method of forming at least one semi-insulating region in a semiconductor substrate, the method comprising:

forming at least one first mask above the semiconductor substrate, the first mask blocking the semi-insulating region;

forming a second mask on a surface of the semiconductor substrate, the second mask covering the semi-insulating region;

implanting the semi-insulating region with a high energy beam of particles by utilizing the second mask and the first mask as particle hindering masks; and

removing the second mask.

[c2] 2.The method of claim 1 wherein the semiconductor substrate comprises a silicon substrate, a germanium substrate, a gallium arsenide substrate, a silicon germanium substrate, an indium phosphide substrate, a gallium nitride substrate, a silicon carbide substrate, or a silicon on insulator (SOI) substrate.

[c3] 3.The method of claim 1 wherein a plurality of nonadja-

cent non-insulating regions are comprised on the surface of the semiconductor substrate.

[c4] 4.The method of claim 3 wherein a plurality of nonadjacent first patterns are defined in the first mask, each first pattern is used for defining the plurality of nonadjacent non-insulating regions.

[c5] 5.The method of claim 4 wherein the first pattern has a plurality of thicknesses.

[c6] 6.The method of claim 3 wherein a plurality of nonadjacent second patterns are defined in the second mask, each second mask is used for defining the plurality of nonadjacent non-insulating regions.

[c7] 7.The method of claim 6 wherein the second pattern has a plurality of thicknesses.

[c8] 8.The method of claim 1 wherein to implant the semi-insulating region with the high energy beam of particles is to damage the structure of the semiconductor substrate to a specific depth in the semi-insulating region so as to increase the resistivity of the semiconductor substrate in the semi-insulating region.

[c9] 9.The method of claim 1 wherein at least one first isolation layer is comprised on the surface of the semicon-

ductor substrate.

[c10] 10.The method of claim 9 wherein at least one active device and at least one passive device are comprised between the surface of the semiconductor substrate and the first isolation layer.

[c11] 11.The method of claim 10 wherein the active device comprises a metal-oxide-semiconductor transistor (MOS transistor), a bipolar junction transistor (BJT), or a power amplifier, and the passive device comprises an antenna, a high quality factor inductor (high Q inductor), a power divider, a filter, a resonator, a transmission line, or a coupler.

[c12] 12.The method of claim 10 wherein the second mask is a composite layer and the composite layer is a stacked structure of a patterned photoresist layer and a second isolation layer from top to bottom.

[c13] 13.The method of claim 12 wherein the second isolation layer comprises a silicon oxide layer (SiO_x layer, $0<x\leq2.0$), a silicon nitride layer (SiN_y layer, $0<y\leq1.33$), or a silicon oxynitride layer (SiO_xN_y layer, $0<x\leq2.0$, $0<y\leq1.33$) formed by a low temperature process.

[c14] 14.The method of claim 13 wherein a multilevel metallization process is performed before forming the second

isolation layer to electrically connect the active device and the passive device to at least one bonding pad, at least one metal line, or at least one interconnect.

[c15] 15.The method of claim 13 wherein a lower level metallization process is performed before forming the second isolation layer, an upper level metallization process is performed after removing the second mask to electrically connect the active device and the passive device to at least one bonding pad, at least one metal line, or at least one interconnect.

[c16] 16.The method of claim 10 wherein a multilevel metallization process is performed after removing the second mask to electrically connect the active device and the passive device to at least one bonding pad, at least one metal line, or at least one interconnect.

[c17] 17.The method of claim 10 wherein at least one third isolation layer is comprised between the semiconductor substrate and the device in the semi-insulating region.

[c18] 18.The method of claim 1 wherein the first mask comprises a patterned dummy wafer or a metal plate formed from a high atomic weight metal material.

[c19] 19.The method of claim 18 wherein the dummy wafer comprises a silicon substrate, a germanium substrate, a

gallium arsenide substrate, a silicon germanium substrate, an indium phosphide substrate, a gallium nitride substrate, a silicon carbide substrate, or a silicon on insulator (SOI) substrate.

[c20] 20.The method of claim 1 wherein the second mask is a patterned photoresist layer.

[c21] 21.The method of claim 1 wherein the high energy particles comprise protons, hydrogen atoms, deuterons, tritons, alpha (α) particles, molecular nitrogen ions, or molecular oxygen ions.

[c22] 22.The method of claim 1 wherein to implant the semi-insulating region with the high energy beam of particles is to make the high energy beam of particles penetrate through the semiconductor substrate outside the semi-insulating region so as to prevent the structure of the semiconductor substrate outside the semi-insulating region from being damaged.

[c23] 23.The method of claim 22 wherein the semiconductor substrate penetrated through by the high energy beam of particles is not insulated.

[c24] 24.A method of forming at least one semi-insulating region in a semiconductor substrate, the method comprising:

forming at least one mask above the semiconductor substrate, the mask blocking the semi-insulating region; and

implanting the semiconductor substrate with a high energy beam of particles by utilizing the mask as a particle hindering mask.

[c25] 25.The method of claim 24 wherein the semiconductor substrate comprises a silicon substrate, a germanium substrate, a gallium arsenide substrate, a silicon germanium substrate, an indium phosphide substrate, a gallium nitride substrate, a silicon carbide substrate, or a silicon on insulator (SOI) substrate.

[c26] 26.The method of claim 24 wherein a plurality of nonadjacent non-insulating regions are comprised on the surface of the semiconductor substrate.

[c27] 27.The method of claim 26 wherein a plurality of nonadjacent patterns are defined in the mask, each pattern is used for defining the plurality of nonadjacent non-insulating regions.

[c28] 28.The method of claim 27 wherein the pattern has a plurality of thicknesses.

[c29] 29.The method of claim 24 wherein to implant the semiconductor substrate with the high energy beam of parti-

cles is to damage the structure of the semiconductor substrate to a specific depth in the semi-insulating region so as to increase the resistivity of the semiconductor substrate in the semi-insulating region.

[c30] 30.The method of claim 24 wherein at least one first isolation layer is comprised on the surface of the semiconductor substrate.

[c31] 31.The method of claim 30 wherein at least one active device and at least one passive device are comprised between the surface of the semiconductor substrate and the first isolation layer.

[c32] 32.The method of claim 31 wherein the active device comprises a metal-oxide-semiconductor transistor (MOS transistor), a bipolar junction transistor (BJT), or a power amplifier, and the passive device comprises an antenna, a high quality factor inductor (high Q inductor), a power divider, a filter, a resonator, a transmission line, or a coupler.

[c33] 33.The method of claim 31 wherein a multilevel metallization process is performed after implanting the semiconductor substrate with the high energy beam of particles to electrically connect the active device and the passive device to at least one bonding pad, at least one

metal line, or at least one interconnect.

[c34] 34.The method of claim 31 wherein a multilevel metallization process is performed before implanting the semiconductor substrate with the high energy beam of particles to electrically connect the active device and the passive device to at least one bonding pad, at least one metal line, or at least one interconnect.

[c35] 35.The method of claim 31 wherein a lower level metallization process is performed before implanting the semiconductor substrate with the high energy beam of particles, and an upper level metallization process is performed after implanting the semiconductor substrate with the high energy beam of particles to electrically connect the active device and the passive device to at least one bonding pad, at least one metal line, or at least one interconnect.

[c36] 36.The method of claim 24 wherein the mask comprises a patterned dummy wafer or a metal plate formed from a high atomic weight metal material.

[c37] 37.The method of claim 36 wherein the dummy wafer comprises a silicon substrate, a germanium substrate, a gallium arsenide substrate, a silicon germanium substrate, an indium phosphide substrate, a gallium nitride

substrate, a silicon carbide substrate, or a silicon on insulator (SOI) substrate.

[c38] 38.The method of claim 24 wherein the high energy particles comprise protons, hydrogen atoms, deuterons, tritons, alpha (α) particles, molecular nitrogen ions, or molecular oxygen ions.

[c39] 39.The method of claim 24 wherein the mask is used to reduce the implantation energy of the high energy beam of particles so as to damage the structure of the semiconductor substrate to a specific depth in the semi-insulating region and to increase the resistivity of the semiconductor substrate in the semi-insulating region.

[c40] 40.The method of claim 24 wherein to implant the semiconductor substrate with the high energy beam of particles is to make the high energy beam of particles penetrate through the semiconductor substrate outside the semi-insulating region so as to prevent the structure of the semiconductor substrate outside the semi-insulating region from being damaged.

[c41] 41.A method of forming at least one semi-insulating region in a semiconductor substrate, the method comprising:

forming a mask on a surface of the semiconductor sub-

strate, the mask covering the semi-insulating region;
implanting the semiconductor substrate with a high energy beam of particles by utilizing the mask as a particle hindering mask; and
removing the mask.

[c42] 42.The method of claim 41 wherein the semiconductor substrate comprises a silicon substrate, a germanium substrate, a gallium arsenide substrate, a silicon germanium substrate, an indium phosphide substrate, a gallium nitride substrate, a silicon carbide substrate, or a silicon on insulator (SOI) substrate.

[c43] 43.The method of claim 41 wherein a plurality of nonadjacent non-insulating regions are comprised on the surface of the semiconductor substrate.

[c44] 44.The method of claim 43 wherein a plurality of nonadjacent patterns are defined in the mask, each pattern is used for defining the plurality of nonadjacent non-insulating regions.

[c45] 45.The method of claim 44 wherein the pattern has a plurality of thicknesses.

[c46] 46.The method of claim 41 wherein to implant the semiconductor substrate with the high energy beam of particles is to damage the structure of the semiconductor

substrate to a specific depth in the semi-insulating region so as to increase the resistivity of the semiconductor substrate in the semi-insulating region.

[c47] 47.The method of claim 41 wherein at least one first isolation layer is comprised on the surface of the semiconductor substrate.

[c48] 48.The method of claim 47 wherein at least one active device and at least one passive device are comprised between the surface of the semiconductor substrate and the first isolation layer.

[c49] 49.The method of claim 48 wherein the active device comprises a metal-oxide-semiconductor transistor (MOS transistor), a bipolar junction transistor (BJT), or a power amplifier, and the passive device comprises an antenna, a high quality factor inductor (high Q inductor), a power divider, a filter, a resonator, a transmission line, or a coupler.

[c50] 50.The method of claim 48 wherein a multilevel metallization process is performed after implanting the semiconductor substrate with the high energy beam of particles to electrically connect the active device and the passive device to at least one bonding pad, at least one metal line, or at least one interconnect.

[c51] 51.The method of claim 48 wherein a multilevel metallization process is performed before implanting the semiconductor substrate with the high energy beam of particles to electrically connect the active device and the passive device to at least one bonding pad, at least one metal line, or at least one interconnect.

[c52] 52.The method of claim 48 wherein a lower level metallization process is performed before implanting the semiconductor substrate with the high energy beam of particles, and an upper level metallization process is performed after implanting the semiconductor substrate with the high energy beam of particles to electrically connect the active device and the passive device to at least one bonding pad, at least one metal line, or at least one interconnect.

[c53] 53.The method of claim 41 wherein the mask is a patterned photoresist layer.

[c54] 54.The method of claim 41 wherein the high energy particles comprise protons, hydrogen atoms, deuterons, tritons, alpha (α) particles, molecular nitrogen ions, or molecular oxygen ions.

[c55] 55.The method of claim 41 wherein the mask is used to reduce the implantation energy of the high energy beam

of particles so as to damage the structure of the semiconductor substrate to a specific depth in the semi-insulating region and to increase the resistivity of the semiconductor substrate in the semi-insulating region.

[c56] 56.The method of claim 41 wherein to implant the semiconductor substrate with the high energy beam of particles is to make the high energy beam of particles penetrate through the semiconductor substrate outside the semi-insulating region so as to prevent the structure of the semiconductor substrate outside the semi-insulating region from being damaged.